CHANGE/ERRATA INFORMATION

ISSUE NO: 3 3/89

This change/errata contains information necessary to ensure the accuracy of the following manual. Enter the corrections in the manual if either one of the following conditions exist:

1. The revision letter stamped on the indicated PCB is equal to or higher than that given with each change.
2. No revision letter is indicated at the beginning of the change/errata.

MANUAL

Title: 9000A-8080
Print Date: June 1981
Rev.- Date: 1-7/81

C/E PAGE EFFECTIVITY

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CHANGE #1 - 15431
Rev.-D, A18 Interface PCB Assembly (9000A-8080-4072T)

On page 6-9, Table 6-3:
ADD: CR6|DIODE, SI, HI-SPEED SWITCHING|313247|28480|HP5082-6264|1

On page 6-11/6-12, Figure 6-3, add CR6 as shown in Figure 1.

On page 7-4, Figure 7-2, add CR6 as shown in Figure 2.

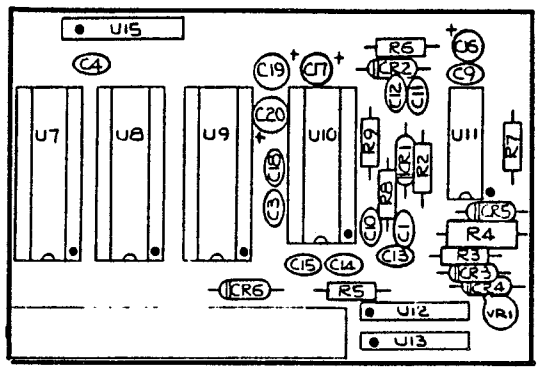

Figure 1.

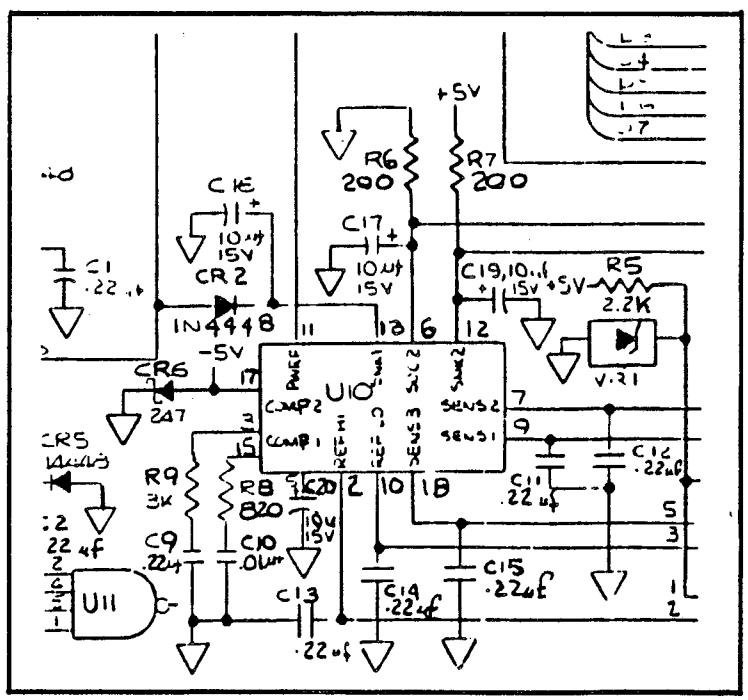

Figure 2.

CHANGE #2 - 15527
Rev.-D, A17 Processor PCB Assembly (9000A-8080-4071T)

On page 6-6, Table 6-2:
ADD: XU16|SOCKET, IC, 14-PIN DIL (NOT SHOWN)
|276527|91506|314-AG39D|1

CHANGE #3 - 16116
Rev.-E, A17 Processor PCB Assembly (9000A-8080-4071T)

On page 6-5, Table 6-2:
CHANGE: U3|IC, MOS, N-CHANNEL 16K BIT|586164|89536|586164|1|1
TO: U3|IC, MOS, N-CHANNEL 16K BIT|540366|89536|540366|1|1

CHANGE #4 - 16245, 16419, 16439
Rev.-F, A17 Processor PCB Assembly (9000A-8080-4071T)

On pages 6-5 and 6-6, Table 6-2:

Change the TOT QTY for R1,
FROM: 2
TO: 1

CHANGE: R3|RES, CEP. CAR, 1K +/-5%, 1/4W|343426|80031|CR251-4-5P1K|REF
TO: R3|RES, DPE. CAR, 4.7K +/-5%, 1/4W
|348821|80031|CR251-4-5P4K7|1

CHANGE: R4|RES, DEP. CAR, 51 +/-5%, 1/4W|414540|80031|CR251-4-5P51E|1
TO: R4|RES, DEP. CAR, 1 +/-5%, 1/4W |357665|80031|CR251-4-5P1E |1

CHANGE: P1|CONNECTOR, PIN |513879|00779|4-870221 |60
TO: P1|CONNECTOR, POST, GOLD|649681|00779|3-87011-2|60

CHANGE: U6|IC, TTL, QUAD, 2-INPUT, POS NAND GATE
|393033|01295|SN74LS00N|3|1
TO: U6|IC, TTL, QUAD, 2-INPUT NAND GATE
|654210|12040|DM74LS00N|3|1

CHANGE: U7|IC, TTL, QUAD, 2-INPUT, POS NAND GATE
|393033|01295|SN74LS00N|REF
TO: U7|IC, TTL, QUAD, 2-INPUT NAND GATE
|654210|12040|DM74LS00N|REF

CHANGE: U16|IC, TTL, QUAD, 2-INPUT, POS NAND GATE
|393033|01295|SN74LS00N|REF
TO: U16|IC, TTL, QUAD, 2-INPUT NAND GATE
|654210|12040|DM74LS00N|REF

On page 7-2, Figure 7-1, change the value of R4,
FROM: 51
TO: 1

CHANGE #5 - 17086
Rev.-E, A18 Interface PCB Assembly (9000A-8080-4072T)

On pages 6-8 thru 6-10, Table 6-3:

Change the TOT QTY for C16,
FROM: 2
TO: 4

ADD: C19,C20|CAP, TA, 10 UF +/-20%, 15V
|193623|56289|196D106X0015A1|REF

On page 6-11/6-12, Figure 6-3, add C19 and C20 as shown in Figure 1.

On page 7-4, Figure 7-2, add C19 and C20 as shown in Figure 2.

CHANGE #6 - 17278
Rev.-B, Final Assembly (9000A-8080-5071)

On page 6-3, Table 6-1:
Change the TOT QTY for H1,
FROM: 2
TO: 3

ADD: MP7|LABEL, STATIC CAUTION|605808|89536|605808|1

ADD: MP8|LABEL, UUT CAUTION|634030|89536|634030|1

ADD: MP9|9000A POD ACCESSORIES
- CABLE, UUT
- LABEL, UUT CAUTION
- PLASTIC BAG
- SOCKET, DIP 40-PIN|582254|89536|582254|1

ADD: MP10|RETAINING CLIP|583260|89536|583260|1

CHANGE: W2|CABLE ASSEMBLY, UUT|604769|89536|604769|1
TO: W2|CABLE ASSEMBLY, UUT|685487|89536|685487|1

On page 6-4, Figure 6-1, add H1 and MP10 as shown in Figure 3.

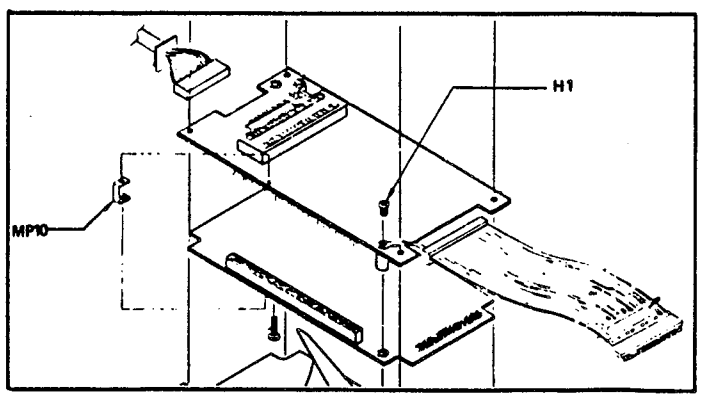

Figure 3.

CHANGE #7 - 17488
Rev.-G, A17 Processor PCB Assembly (9000A-8080-4071T)

On page 6-3, Table 6-1:

CHANGE:	W1	CABLE ASSEMBLY, POD	581827	89536	581827	1
TO:	W1	CABLE ASSEMBLY, POD	581819	89536	581819	1

On pages 6-5 and 6-6, Table 6-2:

DELETE:	R3	.....				
CHANGE:	R4	RES, DEP. CAR, 1 +/-5%, 1/4W	357665	80031	CR251-4-5P1E	1
TO:	R4	RES, DEP. CAR, 39 +/-5%, 1/4W	340836	80031	CR251-4-5P39E	1
CHANGE:	U6	IC, TTL, QUAD 2-INPUT, NAND GATE	654210	12040	DM74LS00N	3 | 1
TO:	U6	IC, FTTL, QUAD 2-INPUT, NAND GATE	654640	07263	74F00PC	1 | 1
CHANGE:	U7	IC, TTL, QUAD 2-INPUT, NAND GATE	654210	12040	DM74LS00N	REF
TO:	U7	IC, TTL, QUAD, 2-INPUT, POS NAND GATE	393033	01295	SN74LS00N	REF
CHANGE:	U16	IC, TTL, QUAD 2-INPUT, NAND GATE	654210	12040	DM74LS00N	REF
TO:	U16	IC, TTL, QUAD, 2-INPUT, POS NAND GATE	393033	01295	SN74LS00N	REF

On pages 6-7, Figure 6-2, delete R3 and add R7 as shown in Figure 4.
On page 7-2, Figure 7-1, delete R3, change the value of R4 to 39 and add R7 as shown in Figure 5.

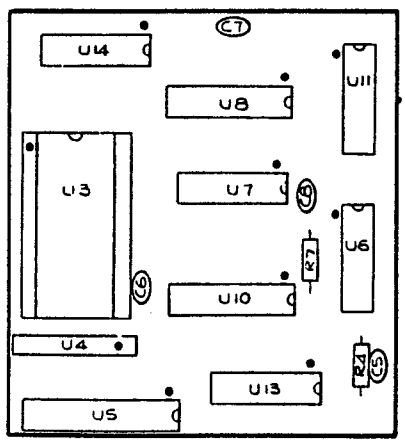

Figure 4.

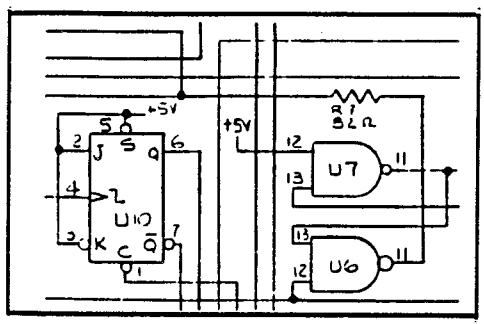

Figure 5.

ERRATA #1

On page 6-3, Table 6-1, make the following changes:

```
CHANGE:   H1|.....................|185918|89536|185918|2
TO:       H1|.....................|185918|COMMERCIAL  |2

CHANGE:   H2|.....................|152132|89536|152132|4
TO:       H2|.....................|152132|COMMERCIAL  |4
```

ERRATA #2

On pages 6-5 and 6-6, Table 6-2, make the following changes:

```
CHANGE:   J4|.....................|512590|89536|512590   |1
TO:       J4|.....................|512590|00779|1-87230-3|1

CHANGE:   MP1|....................|602284|89536|602284      |2
TO:       MP1|....................|602284|9W423|9536B-B-0440|2

CHANGE:   U1|.....................|574905|89536|574905      |1|1
TO:       U1|.....................|574905|91637|MDP1603-202J|1|1
```

ERRATA #3

On page 6-10, Table 6-3, make the following changes:

```
CHANGE:   U15|....................|494690|89536|494690      |1
TO:       U15|....................|494690|91637|CSC06B01472G|1

CHANGE:   VR1|....................|452771|89536|452771 |1|1
TO:       VR1|....................|452771|32293|ITS6935|1|1

CHANGE:   XVR1|...................|175125|89536|175125   |1
TO:       XVR1|...................|175125|07047|10172-DAP|1
```

CAUTION

As noted in the Operator's Manual, it is preferred practice to plug the interface pod into the 9010A mainframe with the pod disconnected from the unit under test and with "power off" in the 9010A mainframe.

In order to activate the pod protection circuitry, turn power-on in the 9010A before plugging the pod into the unit under test.

Form No. F697 8/84